REMARKS

Claims 1-20 and Claim 22 remain pending. New claims 23 and 24 have been added. Claim 22 is amended. Claims 1-20 and Claim 22 stand rejected under 35 USC Section 103 by the Yang reference in combination with Johnson (US 2003 0122696). Applicant requests reconsideration of the rejections in view of the above claim amendments and the arguments presented below.

35 USC Section 103 Rejections

The above referenced Office Action rejects independent Claims 1, 7, and 12 as being rendered obvious by Yang (US 6,553,472) in view of Johnson (US 2003 0122696). Applicant respectfully traverse.

Applicants respectfully point out that the Examiner has the burden of establishing a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2100-126.

With respect to Claim 1, Claim 1 recites:

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>
> A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:
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> generating command signals for accessing an integrated circuit component;
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> accessing data signals for conveying data for the integrated circuit component;
>
> accessing sampling signals for controlling the sampling of the data signals; and
>
> for both data write transactions and data read transactions, automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, wherein the automatic adjusting is free of user input.
>
> ***

Claim 1 recites the limitation that for both data write transactions and data read transactions, the phase relationship adjusting process is accomplished for the command signals, the data signals, and the sampling signals. The calibration of the intra-cycle timing relationships is executed for both data write transactions and data read transactions. Additionally, the adjusting of the phase relationships between the command signals in the data signals and the sampling signals is executed automatically. The phase relationships are automatically adjusted, and this automatic adjusting is free of user input.

Applicant asserts that these limitations are not shown by the Yang reference. Specifically, the Yang reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicant reiterates that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Furthermore, independent Claims 1, 7, and 12 specifically recite the automatic adjusting of the claimed invention is free of user input.

Johnson has been added to show automatic adjusting free of user input as in the claimed invention. Applicant traverses by pointing out that Johnson does not disclose the calibration as in the claimed invention. Johnson does not disclose calibrating for both data write transactions and data read transactions. For example, in the cited paragraph 006 of Johnson, the memory controller is explicitly recited as "achieving this time in calibration at system initialization by sending continuous CCLK and DCLK transitions on the clock paths." Paragraph 006 further states "once a synchronization has been achieved, that is, the proper delays on the data receiving paths have been set, the memory controller stop sending the SYNCH pattern and the SLDRAM, after all calibrations are completed, can be used for normal memory READ and WRITE access." Accordingly, Applicant asserts that Yang does not show the calibration for both data write

transactions and data read transactions as in the claimed invention. Similar limitations are included in each of the independent Claims 7, 12, 18, and 22. Additionally, automatic calibrating and automatic adjusting limitations are included in each of the independent Claims 1, 7, 12, 18, and 22.

Accordingly, Yang in combination with Johnson does not show or suggest the claimed invention as recited in independent Claims 1, 7, 12, 18, and 22 and therefore Claims 1-20 and Claim 22 are not rendered obvious by Yang in combination with Johnson within the meaning of 35 USC Section 103.

With respect to independent Claims 12 and 18, the above referenced Office Action rejects independent Claim 18 as being rendered obvious by Yang in view of Johnson and in view of Suzuki (US 2004/0160833). Applicant respectfully traverses.

As described above, Applicant asserts that Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. The addition of Suzuki does not cure this defect. Suzuki is relied upon for showing a memory controller that controls DDR SDRAM. As with Yang, Suzuki does not show or suggest the automatic calibration and automatic adjusting for both data write

transactions and data read transactions as in the claimed embodiments of the present invention.

Furthermore, applicant points out that Claims 12 and 18 explicitly recites the calibration as taking place without requiring a valid initial operating point within the specified operating parameters for the DRAM component. Applicant points out that the cited section of Yang (e.g., Yang column 2 lines 30-39) does not say anything about inoperative DRAM components. Applicant further point out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope that can support some functional capability of an otherwise nominally inoperative DRAM component. In contrast, such conditions are explicitly recited as within the capabilities of the present invention.

With respect to independent Claim 22, independent Claim 22 has limitations reciting that for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the

DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input.

Independent Claim 22 explicitly adds the limitation stating that the DRAM component that is being calibrated is inoperable at its specified operating parameters. In other words, even though the DRAM device specified as supposedly being operable within a nominal parameter range, within that range it is in fact inoperable. For both data write transactions and data read transactions, the present invention as in Claim 22 can automatically alter the phase relationships to determine some set of parameters that support an operating mode.

Applicant points out that these limitations are not shown or suggested by the Yang reference. As stated above, applicant points out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope double offers some functional capability of an otherwise nominally inoperative DRAM component.

CONCLUSION

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
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